ABSTRACT OF THE DISCLOSURE

In an I/O circuit unit located in the periphery of a semiconductor chip, a plurality of ESD protection transistors are provided in each I/O cell. An electrode pad cell has a two-layer structure including a lower electrode pad and an upper electrode pad. The electrode pad cell is arranged so as to be present over a connection line of ESD protection transistors of an associated I/O cell. With part of the first pad portion of an adjacent electrode pad located in an end portion of the second pad portion of the electrode pad, the second pad portion can not extend further onward but the third pad portion having a smaller width than that of the second pad portion is arranged onward. Thus, destruction of the ESD protection transistors is not caused, so that an internal circuit is protected from an electrostatic discharge which comes into electrode pads.